

Colorado Electronic Product Design

Analog/Digital Design, Telecommunications, DSP, Embedded Systems

User's Manual – Stratix CAS10 Development Board

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Chapter One

Included with this product

With your Stratix CAS10 Development Board you have received the following:

- EP1S10 FPGA Based Development Board
 - with on-board configuration PROM
- Parallel Port Cable
 - allows JTAG configuration directly from a PC
- Floppy Disk with Documentation
 - this manual
 - a reference design to help you get started
- Altera Design Software Starter Suite
 - Includes Quartus II Web Edition

A block diagram of the Stratix CAS10 Development Board is shown below in figure 1. This development board allows rapid prototyping and design verification. Many FPGA pins are available to the user and a through-hole prototyping area is provided for user modifications. There are headers that allow accessory boards to enhance the functions or interface of the development board.

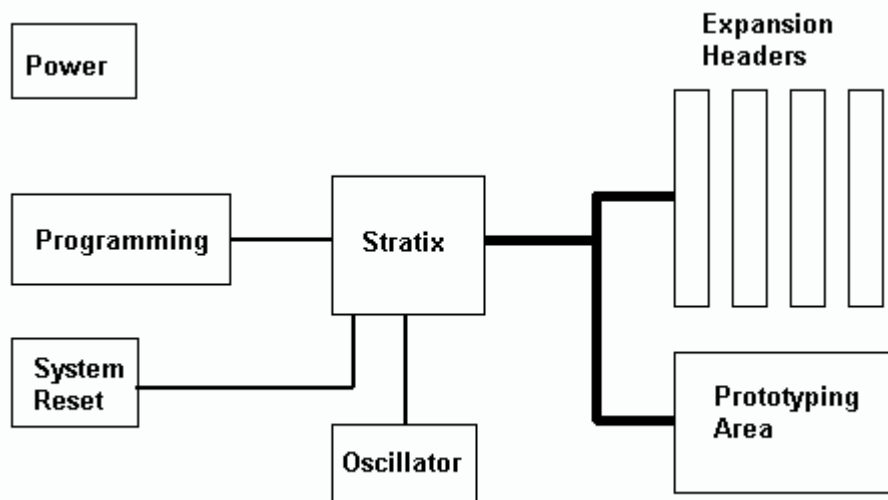


Figure 1. Stratix CAS10 Development Board Block Diagram

Part One – Obtaining Software Tools

All of the software tools necessary to develop and program designs for the Stratix CAS10 Development Board are available free from the Altera website. To download the tools, first go to the Altera website (<http://www.altera.com/>).

- Click on Design Software under the Products header
- Choose Quartus II Web Edition under the By Product section of PLD Designs
- Select Download Quartus II Web Edition Software
- You may now either log in to Altera's web site or register to download
- Download either the single file or multiple file version of Quartus II Web Edition. You should also download Altera's Installation Instructions for reference.
- Before running Quartus II Web Edition, you must also get a license file for running the software. To do this, click on Get A License File. You will now be asked to enter your Network Interface Card (NIC) number. You can get this number from your computer by running a command prompt and typing *ipconfig/all*. The NIC number is the Physical Address of your network card without the dashes. Now enter all remaining information and a license file will be sent to the email address you specified. Save this license file as license.txt in C:\flexlm\ or a directory of your choice.

Part Two – Installation

Once you have downloaded the Quartus II Web Edition installation file, find it on your hard drive and run it. Proceed through the installation and if you have any questions, refer to Altera's installation instructions that you downloaded from Altera's web site. You may be prompted to restart your machine at the end of the installation process. Depending on your operating system, you may need to install additional ByteblasterMV programming drivers. See the Altera's installation instructions for additional information.

Once you have installed the Quartus II Web Edition, make sure that your license file has been found. Start Quartus II Web Edition and go to the Tools menu and select License Setup. If your license file does not appear in the appropriate field, browse for it now. Click Ok.

Part Three – Design Example

Copy the design example from the floppy disk included with your Stratix CAS10 Development Board to your hard drive. Start Quartus II Web Edition and open the example design by selecting File>Open Project from the menu bar.

Part Four – FPGA Configuration

To program the FPGA, make sure that the supplied parallel cable is connected from the printer port of your computer to the header on the Stratix CAS10 Development Board and that the board is powered. In Quartus II Web Edition select Tools->Programmer from the menu bar. Check that the ByteBlaster is selected in the programming hardware box. If not choose Setup, add the ByteBlaster and then Select Hardware. Click on Auto Detect to have Quartus search for the devices on the CAS10. Both the FPGA and the PROM should show up in the list. Right click on device EP1S10 and choose Change File. Select the counter.sof file supplied with the CAS10. Click on the Program/Configure box and then click Start. The configuration done light (D4) comes on when the FPGA has successfully programmed.

Part Five – Functional Test

Once the Stratix CAS10 Development Board has been programmed, the seven segment LED (U8) should be blinking. The output pins on each I/O bank will also be oscillating, indicating the status of the bits of the counter used to divide down the oscillator to generate the seven segment LED pulse.

Part One – Power

External power can be applied to J1 using a transformer with an output between 5V (recommended) and 12V DC or 3.3V and 1.5V power supplies can be applied directly to J2 and J3 respectively. The transformer output should be positive on the tip and negative on the outer ring. LED D6 indicates that the 3.3V supply is powered and D5 indicates that both 3.3V and 1.5V supplies are powered.

Part Two – FPGA I/O Voltage

The EP1S10 runs internally with a voltage of 1.5V but can be configured for a variety of I/O compatibility. The Stratix CAS10 Development Board supports this feature by allowing the user to select the voltage driving the I/O blocks of the FPGA. JP1 allows I/O selection of various blocks before power up. The table below shows what pins of JP1 to connect to give a certain blocks either 1.5V or 3.3V I/O.

I/O Voltage Selection – JP1 Jumper Settings		
I/O Blocks	JP1 pin connection for 1.5V	JP1 pin connection for 3.3V
1 and 2	1-2	2-3
5 and 6	5-6	4-5
7 and 8	7-8	8-9

Part Three – Configuration Options

The configuration options can only be changed by adding and removing certain resistors. It is not recommended that these changes be made and CEPD cannot be responsible for board malfunctions associated with physical modifications.

D4 will light up when configuration is complete.

Part Four – User Reset Options

There are two reset chips on the Stratix CAS10 Development Board. U7 reinitializes the FPGA to be programmed if the 1.5V power supply drops below 1.142V. U6 generates an active-low reset signal to an I/O pin that is held until 200ms after the FPGA has been configured. This signal can also be activated by the push button, SW1.

Part Five – LEDs

There is a 7 segment LED on the Stratix CAS10 Development Board that can be controlled by the user. A logic value of '1' on any of the eight signals will light up the corresponding segment.

There are 3 other LEDs on the board. D4 lights up when configuration is complete. D6 lights up when the 3.3V supply is powered. D5 lights up when both the 1.5V and 3.3V supplies are powered.

Part Six – Miscellaneous

The prototyping area allows direct access to 3.3V, 1.5V, GND, and many FPGA I/O pins. The prototyping area is divided into 14, 2x25 pin headers. These headers are labeled on the board and all signals to these pins are given in the tables in part seven. A square pad on the board represents pin 1.

Part Seven – Accessory Board Header Pin-outs

JP2, JP3, JP4, and JP5 are headers designed to mate with accessory boards to enhance the function and interface of the Stratix CAS10 Development Board. JP6 is a ByteblasterMV input header. JP7 and JP8 represent the signals on the prototyping area. The pin-outs for these headers are shown below.

Accessory Header JP2					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	GND	2	-	VIO3-4
3	B15	B4_B15_CLK12p	4	-	VIO3-4
5	A17	B4_A17_IO	6	B24	B4_B24_IO
7	A12	B3_A12_IO	8	D23	B4_D23_IO
9	C12	B3_C12_IO	10	D22	B4_D22_IO
11	C11	B3_C11_IO	12	C24	B4_C24_IO
13	D11	B3_D11_IO	14	D4	B3_D4_IO
15	A10	B3_A10_IO	16	E22	B4_E22_IO
17	-	GND	18	A15	B4_A15_CLK13p
19	E10	B3_E10_IO	20	B22	B4_B22_IO
21	F10	B3_F10_IO	22	A24	B4_A24_IO
23	G9	B3_G9_IO	24	A22	B4_A22_IO
25	E9	B3_E9_IO_FCLK0	26	C22	B4_C22_IO
27	B9	B3_B9_IO_FCLK1	28	C16	B4_C16_IO
29	D3	B3_D3_IO	30	D16	B4_D16_IO
31	C4	B3_C4_IO	32	H18	B4_H18_IO
33	-	GND	34	B12	B3_B12_CLK14p
35	D12	B3_D12_CLK15p	36	G17	B4_G17_IO_DEV_OE
37	B3	B3_B3_IO	38	AF17	B7_AF17_IO_DEV_CLRn
39	C2	B3_C2_IO	40	F17	B4_F17_IO
41	B4	B3_B4_IO	42	E17	B4_E17_IO
43	D5	B3_D5_IO	44	B17	B4_B17_IO
45	A3	B3_A3_IO	46	G18	B4_G18_IO
47	C3	B3_C3_IO	48	C17	B4_C17_IO
49	-	GND	50	F19	B4_F19_IO

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Accessory Header JP3					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	GND	2	-	VIO1-2
3	N3	B2_N3_CLK0p	4	-	VIO1-2
5	E4	B2_E4_IO	6	N8	B2_N8_IO
7	P6	B1_P6_IO	8	P8	B2_P8_IO
9	P7	B1_P7_IO	10	M9	B2_M9_IO
11	R6	B1_R6_IO	12	M8	B2_M8_IO
13	R7	B1_R7_IO	14	AB4	B1_AB4_IO
15	R8	B1_R8_IO	16	N7	B2_N7_IO
17	-	GND	18	N2	B2_N2_CLK0n
19	R9	B1_R9_IO	20	N6	B2_N6_IO
21	AC3	B1_AC3_IO	22	M5	B2_M5_IO
23	AC4	B1_AC4_IO	24	M4	B2_M4_IO
25	AD1	B1_AD1_IO	26	C1	B2_C1_IO
27	AA2	B1_AA2_IO	28	G6	B2_G6_IO
29	AC2	B1_AC2_IO	30	D2	B2_D2_IO
31	AB3	B1_AB3_IO	32	E3	B2_E3_IO
33	-	GND	34	M1	B2_M1_CLK1p
35	R1	B1_R1_CLK2p	36	K4	B2_K4_IO
37	V5	B1_V5_IO	38	K3	B2_K3_IO
39	V6	B1_V6_IO	40	F3	B2_F3_IO
41	AA3	B1_AA3_IO	42	F4	B2_F4_IO
43	AA4	B1_AA4_IO	44	F1	B2_F1_IO
45	AA1	B1_AA1_IO	46	F2	B2_F2_IO
47	R2	B1_R2_CLK2n	48	G5	B2_G5_IO
49	-	GND	50	R3	B1_R3_CLK3p

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Accessory Header JP4					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	GND	2	-	VIO7-8
3	AE12	B8_AE12_CLK4p	4	-	VIO7-8
5	AB5	B8_AB5_IO	6	AC10	B8_AC10_IO
7	AB16	B7_AB16_IO	8	AB9	B8_AB9_IO_FCLK2
9	AD16	B7_AD16_IO	10	AD9	B8_AD9_IO_FCLK3
11	W17	B7_W17_IO	12	AF12	B8_AF12_IO
13	AE16	B7_AE16_IO	14	AE23	B7_AE23_IO
15	Y17	B7_Y17_IO	16	AD12	B8_AD12_IO
17	-	GND	18	AC12	B8_AC12_CLK5p
19	AC17	B7_AC17_IO_FCLK5	20	AD5	B8_AD5_IO
21	AD17	B7_AD17_IO_FCLK4	22	AD2	B8_AD2_IO
23	AB21	B7_AB21_IO	24	AE2	B8_AE2_IO
25	AE24	B7_AE24_IO	26	AD3	B8_AD3_IO
27	Y18	B7_Y18_IO	28	AE4	B8_AE4_IO
29	AC22	B7_AC22_IO	30	AD4	B8_AD4_IO
31	AC23	B7_AC23_IO	32	AE3	B8_AE3_IO
33	-	GND	34	AF15	B7_AF15_CLK6p
35	AE15	B7_AE15_CLK7p	36	AF3	B8_AF3_IO
37	AB22	B7_AB22_IO	38	AE11	B8_AE11_IO
39	AE22	B7_AE22_IO	40	AB11	B8_AB11_IO
41	AF24	B7_AF24_IO	42	AF10	B8_AF10_IO
43	AF22	B7_AF22_IO	44	AB10	B8_AB10_IO
45	AE25	B7_AE25_IO	46	W10	B8_W10_IO
47	AA17	B7_AA17_IO	48	AA10	B8_AA10_IO
49	-	GND	50	Y10	B8_Y10_IO

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Accessory Header JP5					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	GND	2	-	VIO5-6
3	P24	B6_P24_CLK8p	4	-	VIO5-6
5	AC25	B6_AC25_IO	6	N19	B6_N19_IO
7	C26	B5_C26_IO	8	P19	B6_P19_IO
9	D25	B5_D25_IO	10	R21	B6_R21_IO
11	C25	B5_C25_IO	12	R20	B6_R20_IO
13	D24	B5_D24_IO	14	F23	B5_F23_IO
15	J21	B5_J21_IO	16	P21	B6_P21_IO
17	-	GND	18	R26	B6_R26_CLK9p
19	J22	B5_J22_IO	20	P20	B6_P20_IO
21	E24	B5_E24_IO	22	R23	B6_R23_IO
23	E23	B5_E23_IO	24	R22	B6_R22_IO
25	F26	B5_F26_IO	26	AD25	B6_AD25_IO
27	M21	B5_M21_IO	28	AA25	B6_AA25_IO
29	F25	B5_F25_IO	30	AC24	B6_AC24_IO
31	F24	B5_F24_IO	32	AD26	B6_AD26_IO
33	-	GND	34	P25	B6_P25_CLK9n
35	M26	B5_M26_CLK10p	36	AB24	B6_AB24_IO
37	N20	B5_N20_IO	38	AB23	B6_AB23_IO
39	N21	B5_N21_IO	40	U24	B6_U24_IO
41	M18	B5_M18_IO	42	U23	B6_U23_IO
43	M19	B5_M19_IO	44	AA24	B6_AA24_IO
45	M20	B5_M20_IO	46	AA23	B6_AA23_IO
47	M24	B5_M24_CLK11p	48	AA26	B6_AA26_IO
49	-	GND	50	M25	B5_M25_CLK11n

ByteblasterMV Header JP6					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	TCK	2	-	GND
3	-	TDO	4	-	3.3V
5	-	TMS	6	-	VIO3-4
7	-	No Connect	8	-	No Connect
9	-	TDI	10	-	GND

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Accessory Header JP7					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	-	3.3V	2	AC7	B8_AC7_IO
3	-	3.3V	4	AD6	B8_AD6_IO
5	-	3.3V	6	AE7	B8_AE7_IO
7	-	3.3V	8	AB7	B8_AB7_IO
9	-	3.3V	10	AD7	B8_AD7_IO
11	-	3.3V	12	AE6	B8_AE6_IO
13	-	3.3V	14	AA7	B8_AA7_IO
15	-	3.3V	16	AF7	B8_AF7_IO
17	-	1.5V	18	AF6	B8_AF6_IO
19	-	1.5V	20	Y1	B1_Y1_IO
21	-	1.5V	22	Y2	B1_Y2_IO
23	-	1.5V	24	Y5	B1_Y5_IO
25	-	1.5V	26	Y6	B1_Y6_IO
27	-	1.5V	28	U1	B1_U1_IO
29	-	1.5V	30	L4	B2_L4_IO
31	-	1.5V	32	L5	B2_L5_IO
33	-	GND	34	L2	B2_L2_IO
35	-	GND	36	L3	B2_L3_IO
37	-	GND	38	F13	B9_F13_IO
39	-	GND	40	E13	B9_E13_IO
41	-	GND	42	F14	B9_F14_IO
43	-	GND	44	E14	B9_E14_IO
45	-	GND	46	F12	B9_F12_IO
47	-	GND	48	E12	B9_E12_IO
49	-	GND	50	AB12	B11_AB12_IO

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Accessory Header JP8					
Pin	FPGA Pin	Signal Name	Pin	FPGA Pin	Signal Name
1	E18	B4_E18_IO_FCLK7	2	-	No Connect
3	G19	B4_G19_IO_FCLK6	4	-	No Connect
5	C15	B4_C15_IO_DATA1	6	-	No Connect
7	H16	B4_H16_IO_DATA2	8	-	No Connect
9	F15	B4_F15_IO_DATA3	10	-	No Connect
11	E11	B3_E11_IO_DATA4	12	-	No Connect
13	G11	B3_G11_IO_DATA5	14	-	No Connect
15	H10	B3_H10_IO_DATA6	16	-	No Connect
17	G10	B3_G10_IO_DATA7	18	-	No Connect
19	D10	B3_D10_IO_CLKUSR	20	-	No Connect
21	AC11	B8_AC11_IO_RDYnBSY	22	-	No Connect
23	Y11	B8_Y11_IO_nCS	24	-	No Connect
25	AA11	B8_AA11_IO_CS	26	-	No Connect
27	AA9	B8_AA9_IO_PGM2	28	-	No Connect
29	AC16	B7_AC16_IO_PGM1	30	-	No Connect
31	W15	B7_W15_IO_PGM0	32	-	No Connect
33	E16	B4_E16_IO_nWS	34	-	No Connect
35	Y16	B7_Y16_IO_nRS	36	-	No Connect
37	AD15	B7_AD15_IO_RUnLU	38	-	No Connect
39	AC15	B7_AC15_IO_INIT_DONE	40	-	No Connect
41	AA13	B11_AA13_IO	42	-	No Connect
43	AB13	B11_AB13_IO	44	-	No Connect
45	W12	B8_W12_PLL_ENA	46	-	No Connect
47	AF17	B7_AF17_IO_DEV_CLRn	48	-	No Connect
49	G17	B4_G17_IO_DEV_OE	50	-	No Connect

Part Eight – Board Schematic and Part Placement

The following ten pages show the Stratix CAS10 Development Board schematic. The first four pages show the Stratix FPGA. Page five shows the accessory board headers. Page six contains the programming interfaces. Page seven contains the configuration PROM. The power regulators, reset chips, and oscillator are on page eight. Page nine shows all LEDs and page ten the prototyping area. The last page shows the component placement on the top of the Stratix CAS10 Development Board.